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EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/811,995	ADILETTA ET AL.
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>27 February 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>17-21,23-26,28 and 29</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>17-21, 23-26, and 28-29</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 17-21, 23-26, and 28-29 have been considered. Claims 17, 23, 24, 26, 28, and 29

are amended as per Applicant's request. Claims 22 and 27 have been cancelled as per

Applicant's request.

Papers Submitted

2.   It is hereby acknowledged that the following papers have been received and placed of

record in the file: Amendment as received 27 February 2006.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claims 17-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et

al., U.S. Patent Number 5,663,012 (herein referred to as Shimizu) in view of David K. Probst's

"Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable

Shared-Memory Multiprocessors" from Proceedings of the Twenty-Seventh Annual Hawaii

International Conference on System Sciences, 1994 ©1994 IEEE (herein referred to as Probst).

5.   Referring to claim 17, Shimizu has taught a hardware-based processor comprising:

      a.   Each microengine comprising

            i.   A context event arbiter (Shimizu column 5, line 41 to column 7, line 32;

                    Figure 11; and Figure 12),

        ii.   A controller (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

        iii.   A control store (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

        iv.   Local read and write transfer registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

        v.   Local general purpose registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12), and

        vi.   An arithmetic logic unit (ALU) (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

    b.   Each microengine supporting instructions that perform

        i.   An ALU operation on one or two operands (Shimizu column 4, lines 12-34; column 4, line 51 to column 5; line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17),

        ii.   Deposit a result in a destination register (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17) and

        iii.   Update ALU condition codes according to the result (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to

column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and

Figure 17), and

iv.   A local register instruction that loads one or more bytes, specified by a

field of the instruction representing a mask, within a local destination

register with a shifted value of another operand (Shimizu column 4, lines

12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column

11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure

17).

6.   Shimizu has not taught a multithreaded processor comprising a plurality of microengines.

Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page

585, section 2). A person of ordinary skill in the art at the time the invention was made, and as

taught by Probst, would have recognized that a multithreaded processor tolerates latencies and

increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention was made to

incorporate the multithreaded processor of Probst in the device of Shimizu to improve processor

utilization.

7.   Referring to claim 18, Shimizu has taught wherein the destination register is an absolute

transfer register (Shimizu column 4, lines 35-48 and Figure 8).

8.   Referring to claim 19, Shimizu has taught wherein the destination register is a context-

relative transfer register (Shimizu column 4, lines 35-48 and Figure 8).

9.   Referring to claim 20, Shimizu has taught wherein the destination register is a general-

purpose register (Shimizu column 4, lines 35-48 and Figure 8).

10.   Referring to claim 21, Shimizu has taught wherein the local register instruction comprises

the destination register (Shimizu).

11.   Referring to claim 23, Shimizu has taught wherein the mask is 4-bits (Shimizu column 4,

lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47;

Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

12.   Referring to claim 24, Shimizu has taught wherein the mask comprises a set bit indicating

a corresponding byte in the local register to be loaded (Shimizu column 4, lines 12-34; column 4,

line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure

9; Figure 10; Figure 16; and Figure 17).

13.   Referring to claim 25, Shimizu has taught wherein the local register instruction comprises

a context relative source register (Shimizu column 4, lines 35-48 and Figure 8).

14.   Referring to claim 26, Shimizu has taught an apparatus comprising:

      a.   In a hardware-based processor, each microengine comprising

            i.   A context event arbiter (Shimizu column 5, line 41 to column 7, line 32;

                 Figure 11; and Figure 12),

            ii.   A controller (Shimizu column 5, line 41 to column 7, line 32; Figure 11;

                 and Figure 12),

            iii.   A control store (Shimizu column 5, line 41 to column 7, line 32; Figure

                 11; and Figure 12),

            iv.   Local read and write transfer registers (Shimizu column 5, line 41 to

                 column 7, line 32; Figure 11; and Figure 12),

        v.   Local general purpose registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12), and

        vi.   An arithmetic logic unit (ALU) (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

    b.   Each microengines including a command that causes the ALU to load one or more bytes, specified by a field of the command representing a mask, within a destination register of a selected microengine with a shifted value of another one or more bytes of a source register (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

15.   Shimizu has not taught a multithreaded processor comprising a plurality of microengines. Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page 585, section 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Probst, would have recognized that a multithreaded processor tolerates latencies and increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multithreaded processor of Probst in the device of Shimizu to improve processor utilization.

16.   Referring to claim 27, Shimizu has taught wherein the command comprises a field representing a mask that specifies which byte or bytes of the destination register are affected (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

17.   Referring to claim 28, Shimizu has taught wherein the mask is 4-bits (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

18.   Referring to claim 29, Shimizu has taught wherein the mask comprises a set bit indicating a corresponding byte in the source register to be loaded (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

19.   Claims 17-21 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vincent P. Heuring and Harry F. Jordan's Computer Systems Design and Architecture ©1997 (herein referred to as Heuring) in view of David K. Probst's "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors" from Proceedings of the Twenty-Seventh Annual Hawaii International Conference on System Sciences, 1994 ©1994 IEEE (herein referred to as Probst).

20.   Referring to claim 17, Heuring has taught a hardware-based processor comprising:

     a.   Each microengine comprising

         i.   A context event arbiter (Heuring pages 144-145; Figure 4.1; 166-167; and Figure 4.11),

         ii.   A controller (Heuring pages 144-145; Figure 4.1; 166-167; and Figure 4.11),

         iii.   A control store (Heuring pages 144-145; Figure 4.1; 153-154; Figure 4.5; 166-167; and Figure 4.11),

> iv. Local read and write transfer registers (Heuring pages 144-145; Figure
>
> 4.1; 154-156; and Figure 4.6),
>
> v. Local general purpose registers (Heuring pages 144-145; Figure 4.1;
>
> Figure 4.3; 153; and Figure 4.4), and
>
> vi. An arithmetic logic unit (ALU) (Heuring pages 144-145; Figure 4.1;
>
> Figure 4.3; 157; and Figure 4.7),
>
> b. Each microengine supporting instructions that perform
>
> i. An ALU operation on one or two operands (Heuring pages 157-161),
>
> ii. Deposit a result in a destination register (Heuring pages 157-161) and
>
> iii. Update ALU condition codes according to the result (Heuring pages 38-39
>
> and 286), and
>
> iv. A local register instruction that loads one or more specified bytes within a
>
> local destination register with a shifted value of another operand (Heuring
>
> pages 159-161 and Figure 4.8).

21.   Heuring has not taught a multithreaded processor comprising a plurality of microengines.

Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page

585, section 2). A person of ordinary skill in the art at the time the invention was made, and as

taught by Probst, would have recognized that a multithreaded processor tolerates latencies and

increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention was made to

incorporate the multithreaded processor of Probst in the device of Heuring to improve processor

utilization.

22.   Referring to claim 18, Heuring has taught wherein the destination register is an absolute

transfer register (Heuring pages 69-71, Table 2.8).

23.   Referring to claim 19, Heuring has taught wherein the destination register is a context-

relative transfer register (Heuring pages 69-71, Table 2.8).

24.   Referring to claim 20, Heuring has taught wherein the destination register is a general-

purpose register (Heuring pages 157-161).

25.   Referring to claim 21, Heuring has taught wherein the local register instruction comprises

the destination register (Heuring pages 157-161).

26.   Referring to claim 25, Heuring has taught wherein the local register instruction comprises

a context relative source register (Heuring pages 69-71, Table 2.8).

27.   Referring to claim 26, Heuring has taught an apparatus comprising:

     a.   In a hardware-based processor, each microengine comprising

         i.   A context event arbiter (Heuring pages 144-145; Figure 4.1; 166-167; and

             Figure 4.11),

         ii.   A controller (Heuring pages 144-145; Figure 4.1; 166-167; and Figure

             4.11),

         iii.   A control store (Heuring pages 144-145; Figure 4.1; 153-154; Figure 4.5;

             166-167; and Figure 4.11),

         iv.   Local read and write transfer registers (Heuring pages 144-145; Figure

             4.1; 154-156; and Figure 4.6),

         v.   Local general purpose registers (Heuring pages 144-145; Figure 4.1;

             Figure 4.3; 153; and Figure 4.4), and

         vi.   An arithmetic logic unit (ALU) (Heuring pages 144-145; Figure 4.1;

               Figure 4.3; 157; and Figure 4.7),

     b.   Each microengines including a command that causes the ALU to load one or

          more specified bytes within a destination register of a selected microengine with a

          shifted value of another one or more bytes of a source register (Heuring pages

          159-161 and Figure 4.8),

28.   Heuring has not taught a multithreaded processor comprising a plurality of microengines.

Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page

585, section 2). A person of ordinary skill in the art at the time the invention was made, and as

taught by Probst, would have recognized that a multithreaded processor tolerates latencies and

increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention was made to

incorporate the multithreaded processor of Probst in the device of Heuring to improve processor

utilization.

29.   Claims 22-24 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Vincent P. Heuring and Harry F. Jordan's <u>Computer Systems Design and Architecture</u> ©1997

(herein referred to as Heuring) in view of David K. Probst's "Programming, Compiling and

Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors"

from <u>Proceedings of the Twenty-Seventh Annual Hawaii International Conference on System</u>

<u>Sciences, 1994</u> ©1994 IEEE (herein referred to as Probst), as applied to claims 17 and 26 above,

in view of Shimizu et al., U.S. Patent Number 5,663,012 (herein referred to as Shimizu).

30.   Regarding to claims 22-24 and 27-29, Heuring in view of Probst have not taught

    a.   Wherein the local register instruction comprises a field representing a mask that specifies which byte or bytes of the destination register are affected (Applicant's claim 22);

    b.   Wherein the mask is 4-bits (Applicant's claim 23);

    c.   Wherein the mask comprises a set bit indicating a corresponding byte in the local register to be loaded (Applicant's claim 24);

    d.   Wherein the command comprises a field representing a mask that specifies which byte or bytes of the destination register are affected (Applicant's claim 27);

    e.   Wherein the mask is 4-bits (Applicant's claim 28); and

    f.   Wherein the mask comprises a set bit indicating a corresponding byte in the source register to be loaded (Applicant's claim 29).

31.   Shimizu has taught

    a.   Wherein the local register instruction comprises a field representing a mask that specifies which byte or bytes of the destination register are affected (Applicant's claim 22) (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17);

    b.   Wherein the mask is 4-bits (Applicant's claim 23) (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17);

    c.   Wherein the mask comprises a set bit indicating a corresponding byte in the local register to be loaded (Applicant's claim 24) (Shimizu column 4, lines 12-34;

column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47;

Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17);

d.   Wherein the command comprises a field representing a mask that specifies which

byte or bytes of the destination register are affected (Applicant's claim 27)

(Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column

10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure

16; and Figure 17);

e.   Wherein the mask is 4-bits (Applicant's claim 28) (Shimizu column 4, lines 12-

34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line

47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17); and

f.   Wherein the mask comprises a set bit indicating a corresponding byte in the

source register to be loaded (Applicant's claim 29) (Shimizu column 4, lines 12-

34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line

47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

32.   A person of ordinary skill in the art at the time the invention was made, and as taught by

Shimizu, would have recognized that the incorporating the bit mask increases the speed of the

system and decreases the instruction size (Shimizu column 2, lines 37-42). Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention was made to

incorporate the bit mask of Shimizu in the device of Heuring in view of Probst to increase

system speed and decrease instruction size.

Response to Arguments

33.   Applicant's arguments filed 28 February 2006 have been fully considered but they are not

persuasive. Applicant argues in essence on pages 7-10

> ...nowhere does Shimizu describe any instruction that uses an instruction filed,
>
> representing a mask, to specify which bytes of the destination operand to load
>
> data into. Rather, as explained above, to place a source data into a specific
>
> desired byte of the destination register, it is necessary to execute that GETxx or
>
> PUTxx instruction that would cause source data to be placed into that desired byte
>
> of the destination register...

34.   This has not been found persuasive. A mask is a "pattern of characters, bits, or bytes

used to control the elimination or retention of another pattern of characters, bits, or bytes

(www.dictionary.com "mask" ©2000)." As admitted in Applicant's arguments, the GETxx

instruction "...causes a specific predetermined byte of the source operand to be placed into the

lowest portion of a destination operand..." and the PUTxx instruction "...causes a portion of a

source operand to be placed into a specific predetermined byte position of a destination

operand...". In essence, both instructions control which portion of bits in a portion of the

destination operand is eliminated and replaced with a specific byte of a source operand. The

instructions function exactly as the definition of a mask. With regards to the field of the

instruction, the op-code field representing which instruction it is meets this limitation. Also,

with the PUTxx instruction, the source operand field meets the limitation.

Conclusion

35.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

36.   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

37.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The

examiner can normally be reached on M-T 7:00am-4:30pm.

38.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

39.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
11 May 2006

ERIC COLEMAN
PRIMARY EXAMINER